WHAT IS CLAIMED IS:

1. An electronic instrument comprising:
a memory device; and
strobe signal lines through which a first output strobe signal and a second output strobe signal are transmitted in synchronism with output data from said memory device in the data output operation, the first and second output strobe signals being in complementary relation to each other.

2. The electronic instrument as claimed in claim 1, wherein said memory device has a strobe output buffer that generates the first and second output strobe signals based on a predetermined signal, the first and second output strobe signals being supplied from said strobe output buffer to said strobe signal lines when the output data is output from said memory device.

3. The electronic instrument as claimed in claim 1, wherein the first and second output strobe signals have different levels in a preamble time which is a time period before a head of a cross point train of the first and second output strobe signals, the head of the cross point corresponding to a start of a strobe period of the first and

second output strobe signals.

4. The electronic instrument as claimed in claim 3, wherein the first and second output strobe signals have different levels in a postamble time which is a time period after a cross point of the first and second output strobe signals which cross point corresponds to an end of a strobe period of the first and second output strobe signals.

5. The electronic instrument as claimed in claim 3, wherein the levels of the first and second output strobe signals in the preamble time are set by use of a read command as a trigger.

6. The electronic instrument as claimed in claim 3, wherein the levels of the first and second output strobe signals in the preamble time are set a predetermined time before a first output data item is output.

7. The electronic instrument as claimed in claim 6, wherein transistors of said memory device which transistors drive the strobe signal lines are controlled to be in a off state in a

waiting time period.

8. The electronic instrument as claimed in claim 1, wherein each of cross points of the first and second output strobe signals is set at an edge trigger point of a corresponding one of output data items.

9. The electronic instrument as claimed in claim 1, wherein each of cross points of the first and second output strobe signals is set at a center point of a corresponding one of output data items.

10. An electronic instrument comprising:

a memory device; and

strobe signal lines through which a first input strobe signal and a second input strobe signal are transmitted in synchronism with input data supplied to said memory device in the data input operation, the first and second input strobe signals being in complementary relation to each other.

11. The electronic instrument as claimed in claim 10, wherein said memory device has a strobe

input buffer that receives the first and second input strobe signals transmitted through said strobe signal lines and generates, based on the first and second input strobe signals, a strobe clock signal used to settle input data items supplied to said memory device.

12. The electronic instrument as claimed in claim 10, wherein the first and second input strobe signals have different levels in a preamble time which is a time period before a head of a cross point train of the first and second input strobe signals, the head of the cross point corresponding to a start of a strobe period of the first and second input strobe signals.

13. The electronic instrument as claimed in claim 12, wherein the first and second input strobe signals have different levels in a postamble time which is a time period after a cross point of the first and second input strobe signals which cross point corresponds to an end of a strobe period of the first and second input strobe signals.

14. The electronic instrument as claimed in claim 12, wherein the levels of the first and second input strobe signals in the preamble time are set by use of a write command as a trigger.

15. The electronic instrument as claimed in claim 12, wherein the levels of the first and second input strobe signals in the preamble time are set a predetermined time before a first input data item is received.

16. The electronic instrument as claimed in claim 15, wherein transistors of a unit supplying the input data to said memory device which transistors drive the strobe signal lines are controlled to be in a off state in a waiting time period.

17. The electronic instrument as claimed in claim 10, wherein each of cross points of the first and second input strobe signals is set at an edge trigger point of a corresponding one of input data items.

18. The electronic instrument as claimed in claim 10, wherein each of cross points of the first and second input strobe signals is set at a center point of a corresponding one of input data items.

19. An electronic instrument comprising:

a memory device; and

strobe signal lines through which a first output strobe signal and a second output strobe signal are transmitted in synchronism with out put data from said memory device in a data output operation and a first input strobe signal and a second input strobe signal are transmitted in synchronism with input data supplied to said memory device in a data input operation, the first and second output strobe signals being in complementary relation to each other, the first and second input strobe signals being in complementary relation to each other.

20. The electronic instrument as claimed in claim 19, said memory device comprises:

a strobe output buffer that generates the first and second output strobe signals based on a predetermined signal, the first and second output strobe signals being supplied from said strobe output buffer to said strobe signal lines when the output data is output from said memory device; and

a strobe input buffer that receives the first and second input strobe signals transmitted through said strobe signal lines and generates, based on the first and second input strobe signals, a strobe clock signal used to settle input data items supplied to said memory device.

21. The electronic instrument as claimed

in claim 15, wherein the first and second output strobe signals have different levels in a first preamble time which is a time period before a head of a cross point train of the first and second output strobe signals, the head of the cross point corresponding to a start of a strobe period of the first and second output strobe signals, and wherein the first and second input strobe signals have different levels in a second preamble time which is a time period before a head of a cross point train of the first and second input strobe signals, the head of the cross point corresponding to a start of a strobe period of the first and second input strobe signals.

17 18. The electronic instrument as claimed in claim 21, wherein the first and second output strobe signals have different levels in a first postamble time which is a time period after a cross point of the first and second output strobe signals which cross point corresponds to an end of a strobe period of the first and second output strobe signals, and wherein the first and second input strobe signals have different levels in a second postamble time which is a time period after a cross point of the first and second input strobe signals which cross point corresponds to an end of a strobe period of the first and second input strobe signals.

18 19. The electronic instrument as claimed in claim 22, wherein said strobe signal lines

includes output strobe signal lines through which the first and second output strobe signals and input strobe signal lines through which the first and second input strobe signal lines, said output strobe signal lines and said input strobe signal lines being separated from each other, wherein when an even number of consecutive output data items are output, the levels of the first and second output strobe signals are controlled in a waiting time period to be maintained at the same levels as in the first postamble time, and wherein when an even number of consecutive input data items are supplied, the levels of the first and second input strobe signals are controlled in a waiting time period to be maintained at the same levels as in the second postamble time.

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24. The electronic instrument as claimed in claim 22, wherein said strobe signal lines includes output strobe signal lines through which the first and second output strobe signals and input strobe signal lines through which the first and second input strobe signal lines, said output strobe signal lines and said input strobe signal lines being separated from each other, wherein when an odd number of consecutive data output items are output, the levels of the first and second output strove signals are controlled in a waiting time period to be maintained at the same levels as in the first postamble time and then restored at the start of the second preamble time in the next data read operation.

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25. A semiconductor memory device provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data output operation for said semiconductor memory device, and strobe signal lines through which a first output strobe signal and a second output strobe signal are transmitted to be used to settle output data from said semiconductor memory device in the data output operation, the first and second output strobe signals being in complementary relation to each other, said semiconductor memory device comprising:

a data output buffer that outputs the output data from a memory bank; and

a strobe output buffer that generates the first and second output strobe signals based on a predetermined signal, the first and second output strobe signals being supplied from said strobe output buffer to said strobe signal lines when the output data is output from said data output buffer.

26. A semiconductor memory device provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data input operation for said semiconductor memory device, and strobe signal lines through which a first input strobe signal and a second input strobe signal are transmitted to be used to settle input data supplied to said semiconductor memory device in the data input operation, the first and second input strobe signals being in complementary relation to each other, said semiconductor memory device comprising:

a strobe input buffer that receives the first and second input strobe signals transmitted through said strobe signal lines and generates a strobe clock signal based on the first and second input strobe signals; and

a data input buffer that receives input data items supplied to said semiconductor memory device, the input data items being settled by using the clock strobe signal generated by said input strobe buffer.

27. A semiconductor memory device provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data output operation and a data input operation for said semiconductor memory device, and strobe signal lines through which a first output strobe signal, a second output strobe signal, a first input strobe signal and a second input strobe signal are transmitted to be used to settle output data from said memory device in the data output operation and to settle input data supplied to said semiconductor memory device, the first and second output strobe signals being in complementary relation to each other, the first and second input strobe signals being in complementary relation to each other, said memory device comprising:

a data output buffer that outputs the output data from a memory bank;

a strobe output buffer that generates the first and second output strobe signals based on a predetermined signal, the first and second output strobe signals being supplied from said strobe

output buffer to said strobe signal lines when the output data is output from said data output buffer;

a strobe input buffer that receives the first and second input strobe signals transmitted through said strobe signal lines and generates a strobe clock signal based on the first and second input strobe signals; and

a data input buffer that receives input data items supplied to said semiconductor memory device, the input data items being settled by using the clock strobe signal generated by said input strobe buffer.